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SEP 78 R E YEATS, S H CHIAO DAAB07-78-C-2402
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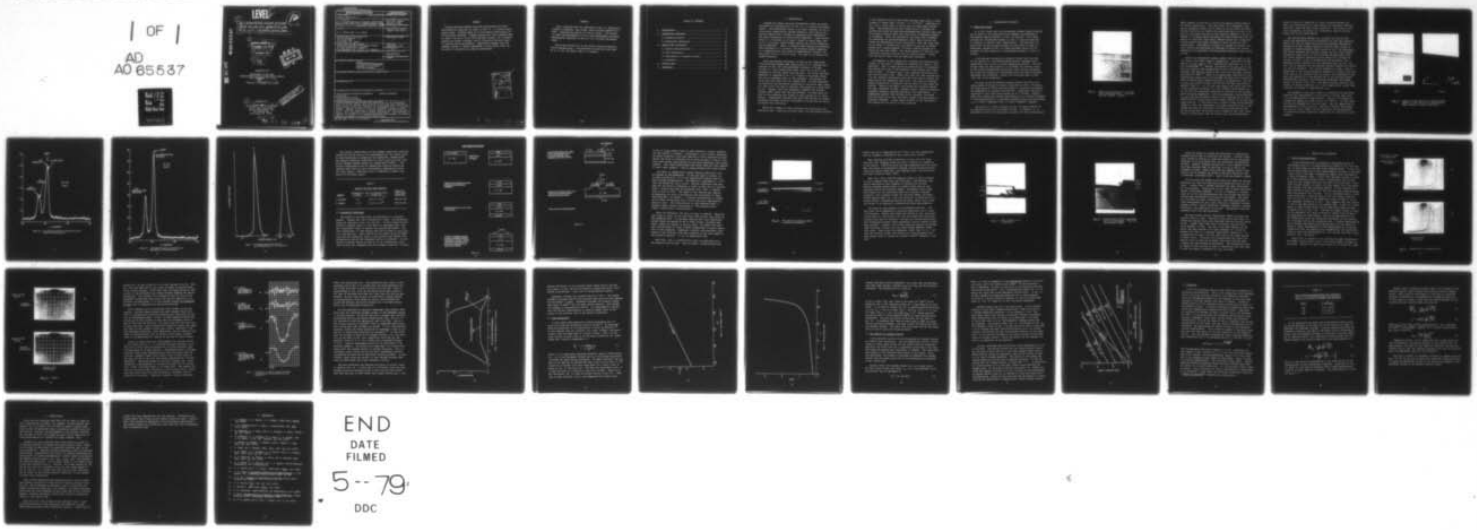

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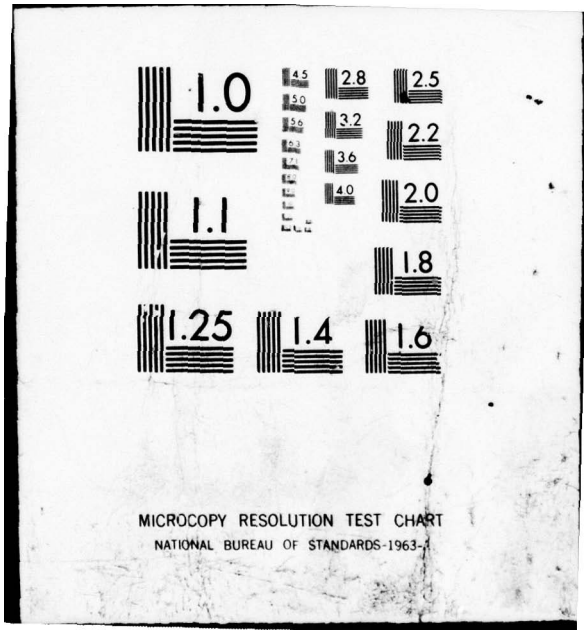
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III-V HETEROSTRUCTURE AVALANCHE PHOTODIODE MODULES FOR FIBER OPTIC COMMUNICATION LINKS IN THE 1.0 TO 1.3 MICROMETER SPECTRAL RANGE.

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Lattice-matched InGaAsP APDs have been grown on InP substrates. Gains of 15 and quantum efficiencies of 63% have been observed on these diodes, which are sensitive to wavelengths up to 1.3 μm and beyond. Leakage current at half the breakdown voltage is below 5×10^{-6} A/cm^2 but increases to higher values in the avalanche gain region, and ultimately limits device performance. The increase in leakage is thought to be surface-dominated and attempts are being made to eliminate it by building guard rings.

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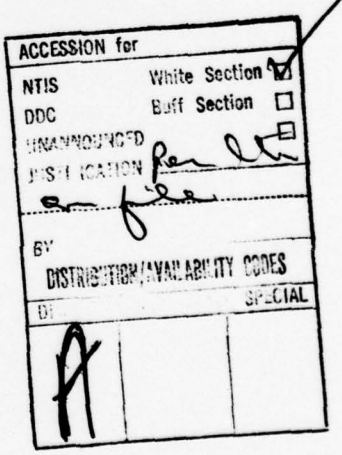
SUMMARY

Lattice-matched InGaAsP avalanche photodiodes have been fabricated for detection of light in the 1.0 - 1.3 micron wavelength range. Uniform gains of 15 and quantum efficiencies of 63% have been achieved. Leakage current for 7-mil diameter APDs is under 5 nA until 70% of the breakdown voltage, but increases rapidly for higher voltages, and is ultimately the main cause of limited device performance. Experiments suggest that the leakage current is surface dominated, so that guard rings can be built to substantially improve performance.



PREFACE

The work reported here was supported by the U.S. Electronics Command, Fort Monmouth, New Jersey, under contract DAAB07-78-C-2402. The Contracting Officer is Claire Loscoe. The program is aimed the development of III-V high performance avalanche photodiod for detection in the 1.0 to 1.3 micron wavelength range.

The work was carried out in the Varian Corporate Research Solid State Laboratory. Contributions to this work were made by R. E. Yates, S-H Chiao, and G. A. Antypas.

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1. INTRODUCTION

InGaAsP and InGaAs avalanche photodiodes (APDs) are being developed for photodetection in the 1.0 - 1.3 micron wavelength region. This wavelength region is of great interest for use in fiber-optic communication systems because in this region the optical fibers have a minimum of dispersion and attenuation.[1] The lower attenuation is particularly important. Fiber attenuation at 1.3 microns is at least a factor of three lower than at 0.8 -0.9 micron (where AlGaAs sources and silicon detectors may be employed). Hence, if equally good sources and detectors were available at 1.3 microns, the distance between repeaters in a communications link would be approximately tripled, e.g. from about 10 km to 30 km or more. Our goal is to develop the needed detectors.

Using preliminary structures, we have so far fabricated lattice-matched InGaAsP APDs having gains of 15, quantum efficiencies of 63%, and 3-dB bandwidths in excess of 50 MHz. (50 MHz is a very conservative lower limit and is due to the bandwidth of the LED source that was used. The actual detector bandwidth is expected to be 1 or 2 orders of magnitude larger and will be measured later in this program.) Preliminary results have also shown gain for InGaAs APDs. We have developed our materials and processing technology to the point where gains of a few (2-10) are easy to achieve, with yields on a good wafer of 75%. However, both the quaternary (InGaAsP) and ternary (InGaAs) APDs suffer from the same problem: too much dark current in the avalanche gain region of bias (though not at lower biases). Experiments indicate that this dark current is surface dominated and hence could be eliminated in future work by building guard ring structures.

There are a number of steps involved with fabricating and testing an APD. Typically we start with a low dislocation density

p^+-InP substrate and by liquid phase epitaxy (LPE) grow a n-type InGaAsP or InGaAs layer, having $n \approx 2 \times 10^{16}/cm^3$. Sometimes we will grow a n-InP layer on top of this by vapor phase epitaxy (VPE). The heterojunction thus formed acts to increase the quantum efficiency by repelling photogenerated carriers away from the external surface where they would have an enhanced tendency to recombine. After the epilayer(s) are grown their bandgaps are determined by photoluminescence, while their lattice constants are determined by x-ray scattering. Next the layer side of the wafer is covered with SiO_2 and/or Si_3N_4 and is vacuum sealed into a quartz ampoule, to which a few milligrams of P and/or As have been added. The sealed ampoule is then put into a diffusion furnace to drive the p-n junction about 1 micron into the active layer from the substrate interface.

The ampoule is then opened and a cleaved and stained cross-section of the wafer is examined to determine the depth of the diffusion. Next a broad area Au-Zn metallization is evaporated and alloyed onto the p^+-InP substrate, thus forming the p-type ohmic contact. Following this, 3-mil diameter Au-Sn dots are put onto the layer side. These 3-mil dots are then covered with 6-12 mil diameter photoresist dots which are used to define the mesas during the subsequent mesa etch. The resist is removed, surface passivation is applied, and the wafer is then ready for testing. While on the wafer, the diodes are typically tested for gain, breakdown voltage, leakage current, series resistance, frequency response, quantum efficiency, and capacitance. If frequencies greater than 200 MHz are of interest, the wafer would be diced up so that individual diodes could be mounted in microwave packages. A more detail account of the fabrication and testing will be given in later sections.

2. FABRICATION PROCEDURE

2.1 Materials Growth

It is well known that lattice-matched InGaAsP heterojunctions can be grown on InP substrates with bandgaps corresponding to wavelengths ranging between 0.9 and 1.65 microns. This range includes the wavelengths between 1.0 and 1.3 microns which are of interest in optical fiber communication. The materials research part of this program focuses on the growth, by LPE, of quaternary InGaAsP as well as InGaAs epilayers which will be suitable for APDs sensitive to wavelengths between 1.0 and 1.3 microns.

A conventional multiple-bin graphite slider boat was used for the growth in a resistance-heated furnace equipped with a sodium heat pipe to get a uniform temperature profile. The substrates were cut from either Zn or Sn-doped InP crystals grown by the liquid encapsulated Czochralski (LEC) pulling technique. The wafers were lapped and chem-mechanically polished to desired smoothness and thickness. Growth runs have been made on both (100) and (111)B substrates.

For most of the quaternary epilayer growth, the melts are single phase solutions critically saturated at 650°C. The melts are supercooled to 640°C and then growth is initiated by bringing the substrate into contact with the melt. Additional cooling is continued at very slow rates ranging up to 0.1°C/min. Figure 1 shows the cleaved and stained cross-section of a p^+-InP/n^--InGaAsP/n^+-InP heterostructure. Different structures have also been grown, e.g. n^+-InP/n^--InGaAsP/p^+-InP, n^+-InP/p^+-InGaAsP/n^--InGaAsP.

The control of layer thickness as well as doping density is an important factor in the design of APDs. In general, it is desirable to have very high purity epilayers so that intentionally

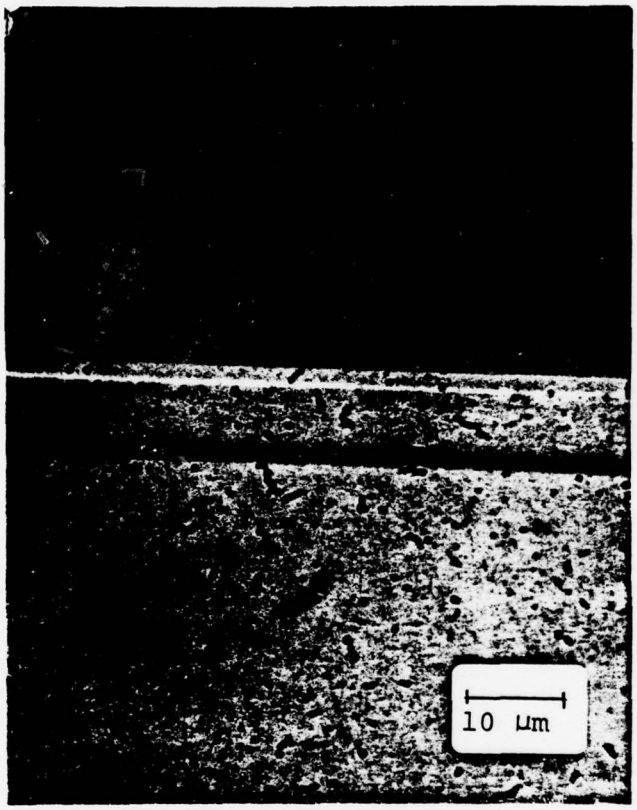


Fig. 1. Etched cross-section of a double layer heterostructure, (100) LPE InP/LPE InGaAsP (1400x).

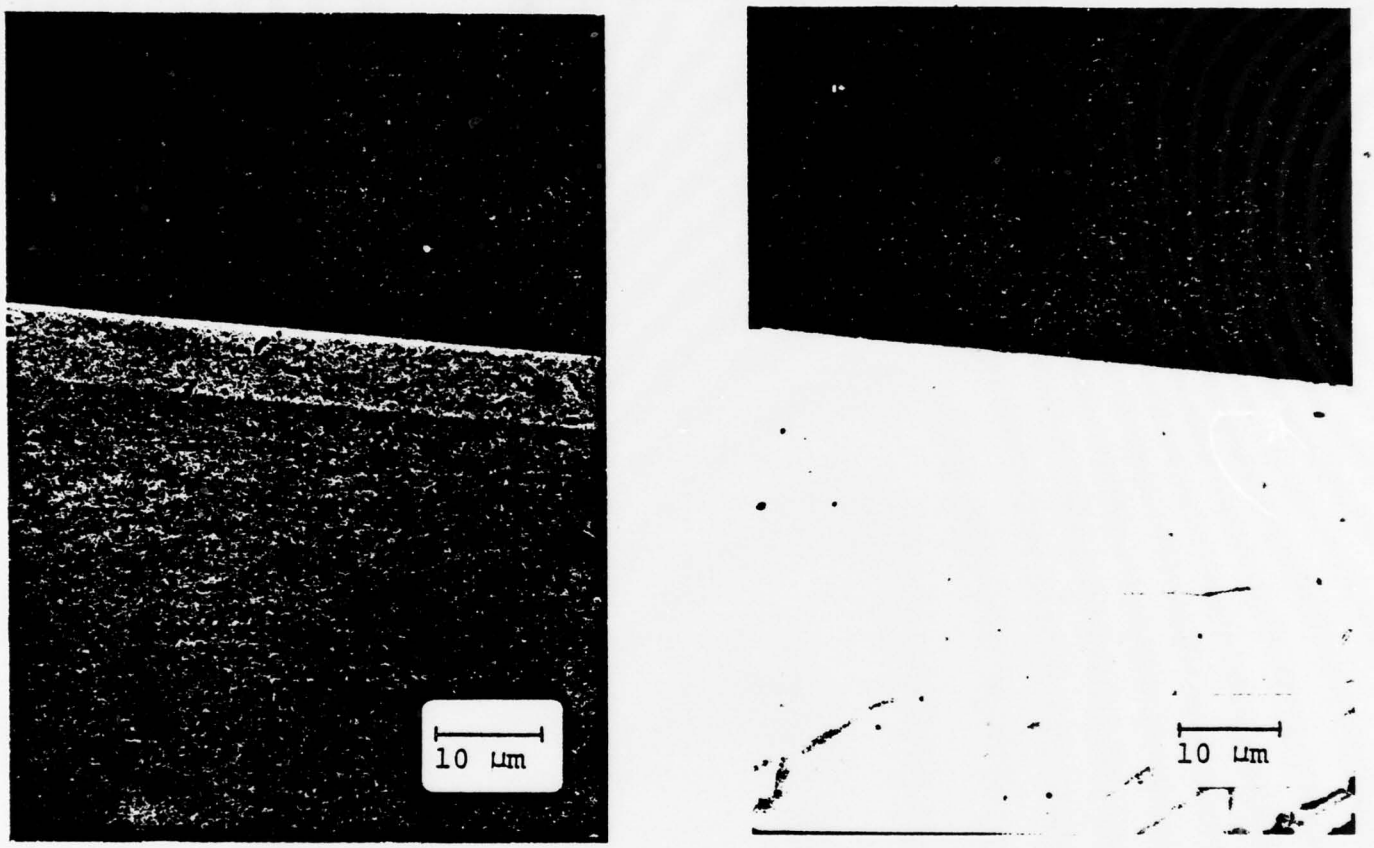
added dopants can be used to achieve the desired doping density for device application. Like many other III-V compounds, high purity quaternary layers can be grown on InP by baking the melts. The main difficulty in baking the quaternary melts is that it is hard to anticipate the loss of the volatile components, As and P. However, a reliable baking procedure has been established for the growth of relatively high purity InGaAsP layers with controlled carrier density and layer thickness on both (111)B and (100) orientations. The effects of baking on bandgap and lattice constant shifts were monitored and analyzed to design the correct composition for perfectly lattice-matched quaternary layer growth on InP.

Unlike the InGaAsP/InP system, InGaAs could be grown on InP over only a very small range of composition. LPE growth of high quality $In_{.53}Ga_{.47}As$ on (111)-oriented InP substrates is by now well established.[3-6] However, LPE growth of $In_{.53}Ga_{.47}As$ on InP has only recently been accomplished on the (100) orientation,[7,8] although high quality growth on the (100) face had been achieved previously by VPE.[6,9] There is an appreciable difference in the distribution coefficient of Ga between the above two orientations, hence different melt compositions had to be determined. For the $In_{.53}Ga_{.47}As$ growth we have utilized the technique described by Pearsall (Ref. 8). All $In_{.53}Ga_{.47}As$ layers were grown from critically saturated solutions, i.e. all solution constituents (In, Ga, and As) are completely dissolved in the bath at the predetermined liquidus temperature. With this technique, lattice-matched $In_{.53}Ga_{.47}As$ was routinely grown on (100)-oriented InP at 630°C from an In melt containing 0.02775 atomic fraction of Ga and saturated with As. It was found that in order to grow lattice-matched InGaAs on (100) InP substrates, the atomic fraction of Ga in the InGaAs melt must be controlled to within one part per million. We also found that the growth rate of InGaAs on the (100) orientation is much faster than the rate on the (111)B orientation.

Figure 2 shows the comparison of layer thickness between the above two orientations for layers grown from nominally identical solutions, under the same growth conditions. The layers on the (100) orientation are grown to a thickness of about 8 microns during the 30 min growth period.

The lattice-match between the epilayers and the InP substrate was determined by x-ray diffraction of the CuKα radiation. Figure 3(a) and (b) shows the diffraction patterns obtained by reflection of CuKα doublet radiation from the (600) planes of InGaAsP or InGaAs epitaxial layers grown on (100) InP substrates. The curves represent the lattice constant of two 1.0-eV bandgap quaternary layers grown on (100)-oriented InP substrates from two almost identical quaternary melts except for a slight difference (0.004%) in the Ga concentration of the melts. The measured lattice constant for the mismatched layer in Fig. 3(a) was 5.872 Å compared with the measured lattice constant of 5.869 Å for the InP substrate. The lattice-mismatch is 0.05%. This is comparable to the lattice parameter mismatch of 0.048% in the commonly used $Al_{.3}Ga_{.7}As$-GaAs laser structure, and considerably less than the mismatch of 0.10% measured for $Al_{.5}Ga_{.5}As$-GaAs system. Nevertheless, perfectly lattice-matched quaternary and InGaAs layers, as shown in Fig. 3(b), have been routinely grown by optimizing the growth conditions (i.e. melt compositions, growth temperatures, and amount of supercooling, etc.).

The bandgaps of the grown layers are determined by photoluminescence (PL) measurements at 77°K using a 0.5-W Ar laser with a S-1 photomultiplier or PbS detector. Typical 77°K spectra of InGaAsP and InGaAs are shown in Fig. 4(a) and (b). At room temperature the bandgaps are 0.065 eV lower. The low temperature PL measurements not only serve as a vehicle to monitor the bandgap but also as a very useful tool for detecting the incorporation of radiative shallow impurities (especially Zn) during the growth process.



(100) (111)B

Fig. 2. Cleaved cross-sections of InGaAs layers grown on (100) and (111)B orientations using identical growth conditions.

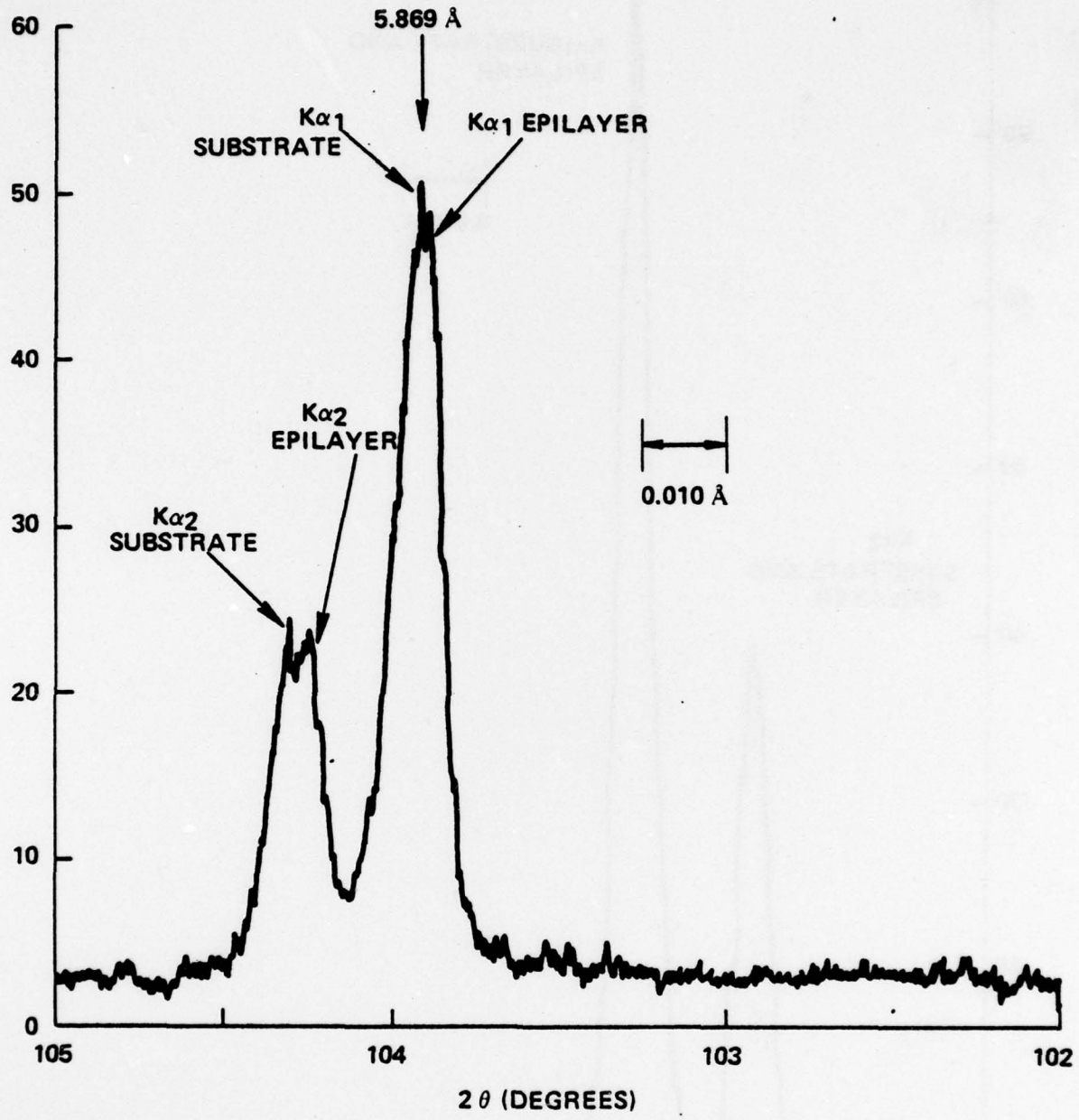


Figure 3(a). CuKα diffraction patterns of (600) planes for layers grown on (100) InP substrates.

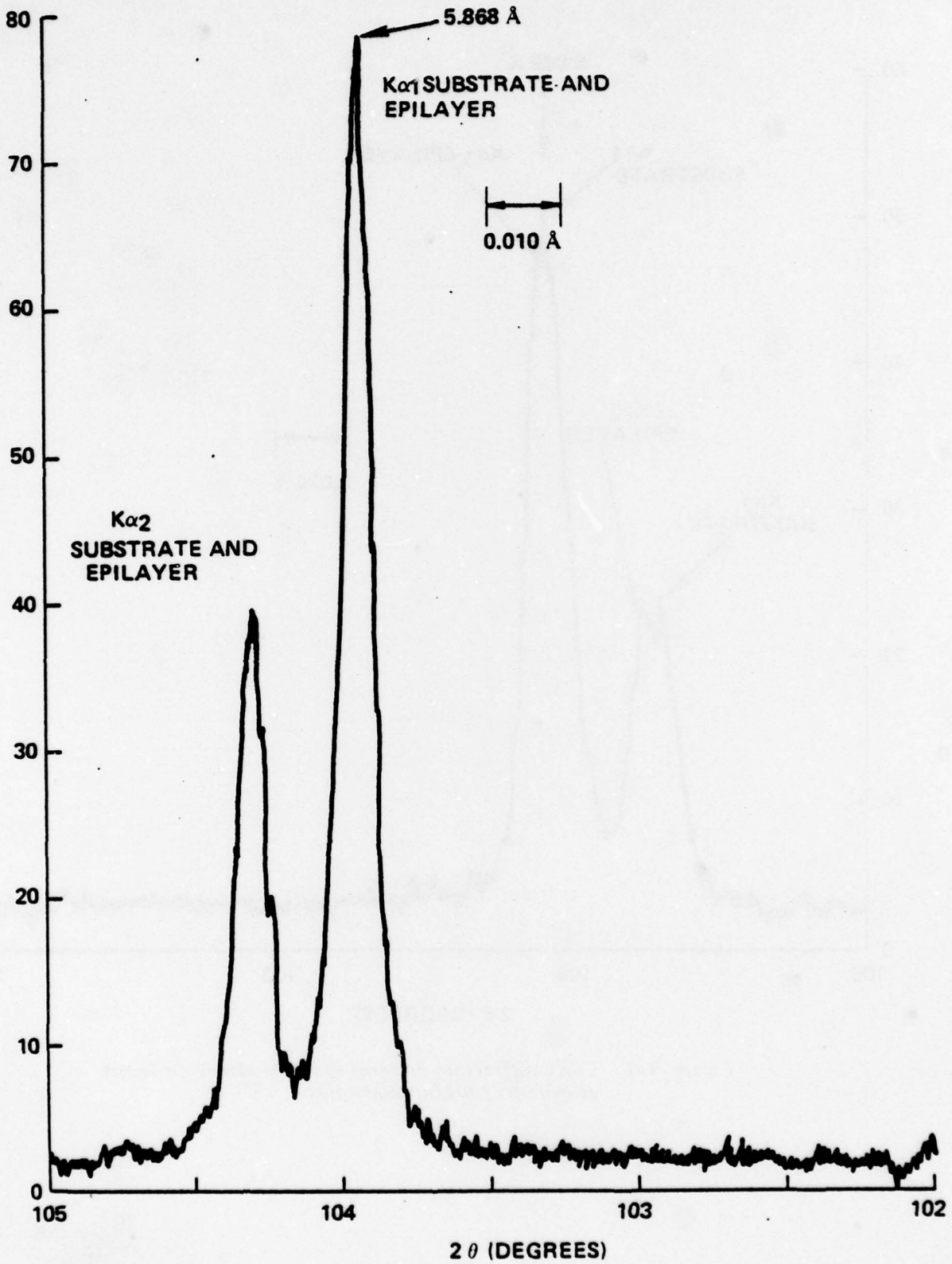


Figure 3(b). CuKα diffraction patterns of (600) planes for layers grown on (100) InP substrates.

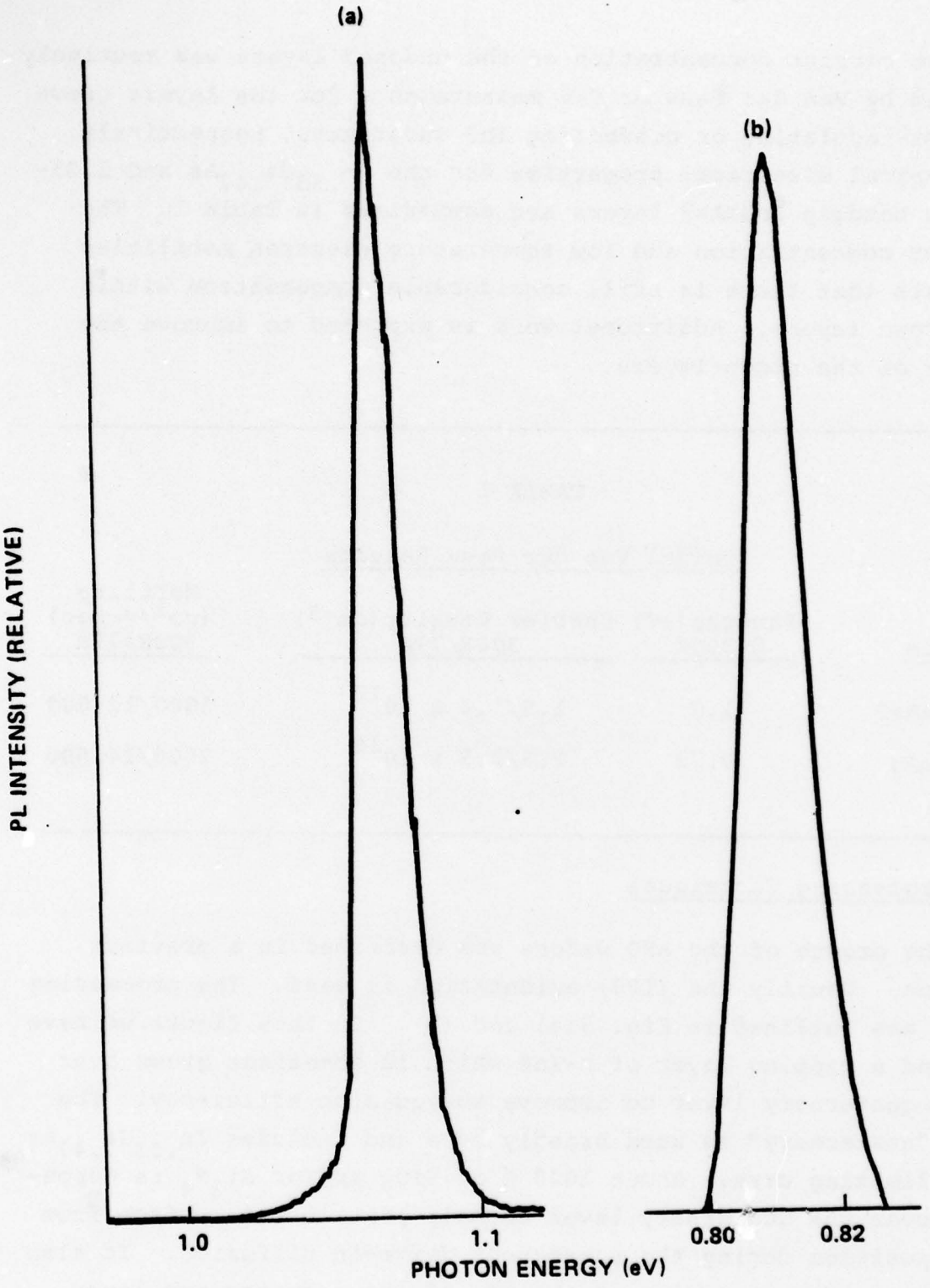


Figure 4. Photoluminescence spectrum at 77°K. (a) An InGaAsP layer; (b) An InGaAs layer.

The carrier concentration of the undoped layers was routinely checked by Van der Pauw or C-V measurements for the layers grown on semi-insulating or conducting InP substrates, respectively. The typical electrical properties for the $In_{.53}Ga_{.47}As$ and 1.25-micron bandgap InGaAsP layers are summarized in Table I. The carrier concentration and low temperature electron mobilities indicate that there is still considerable compensation within the grown layers. Additional work is expected to improve the purity of the grown layers.

TABLE I

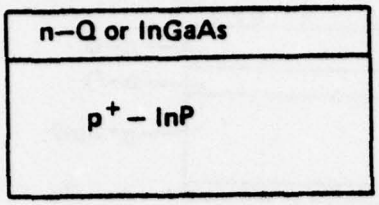
Typical Van der Pauw Results

Sample	Bandgap(eV) @ 300K	Carrier Density(cm^{-3}) 300K/77K	Mobility (cm^2/V-sec) 300K/77K
n-InGaAsP	1.0	$1.5/1.2 \times 10^{16}$	3800/12,000
n-InGaAs	0.72	$2.5/2.5 \times 10^{16}$	7500/14,500

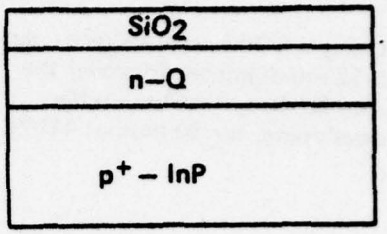
2.2 Processing Techniques

The growth of the APD wafers was described in a previous section. Usually the (100) orientation is used. The processing steps are outlined in Fig. 5(a) and (b). In this figure we have omitted a capping layer of n-InP which is sometimes grown over the n-quaternary layer to improve the quantum efficiency. The term "quaternary" is used broadly here and includes $In_{.53}Ga_{.47}As$ as a limiting case. About 1000 Å of SiO_2 and/or Si_3N_4 is deposited over the quaternary layer to help protect the surface from decomposition during the subsequent drive-in diffusion. It also serves to prevent doping of the top of the n-quaternary layer from Zn which has outgassed from the Zn-doped substrate. Without

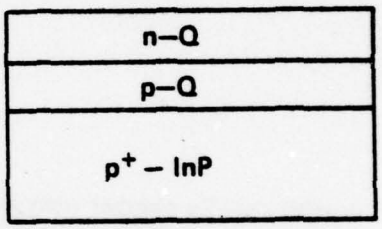
APD FABRICATION STEPS



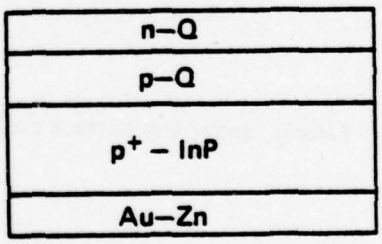
Deposit SiO_2 (or Si_3N_4)



Vacuum seal in ampoule for drive-in diffusion; remove SiO_2 upon completion.



Evaporate and alloy Au–Zn to form p-type contact.



Define 3-mil diameter openings in Shipley AZ1350J photoresist. Evaporate Au–Sn layer. Dissolve resist and lift off excess Au–Sn leaving 3-mil diameter Au–Sn dots on 20-mil centers.

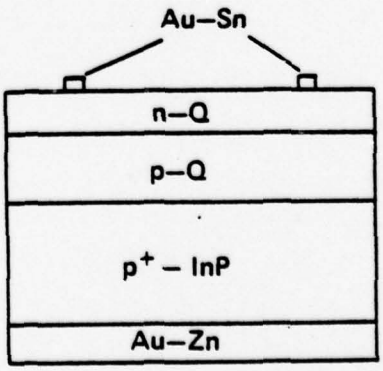
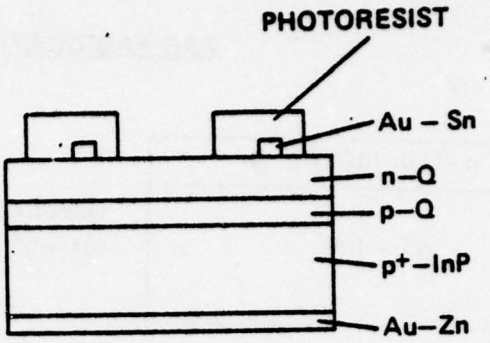
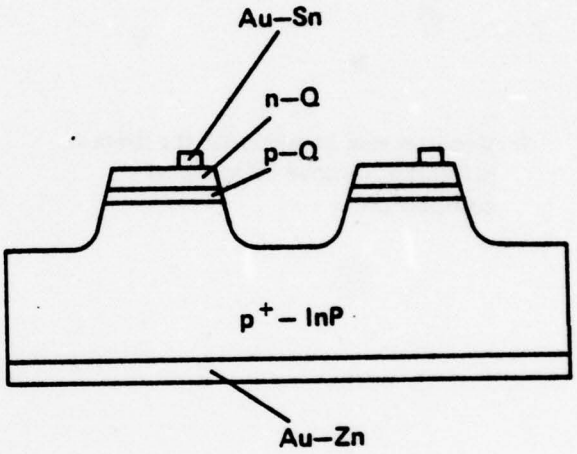


Figure 5 (a)

Using KTI752 negative resist, define 6-12 mil diameter dots over the Au—Sn dots. Post-bake, after developing, for 30 min. at 120°C.



Protect Au—Zn contact with wax and etch mesas with 2% Br-methanol. Remove wax and photoresist.



Finally, apply any surface passivation.

Figure 5 (b)

a SiO_2 or Si_3N_4 capping layer we have observed a greater tendency for the surface to degrade. Furthermore, native oxides (deposited by anodic oxidation) have been observed to cause excessive pitting during the drive-in diffusion and in fact are seen to cause a visible oxide growth (and pitting) on any other previously bare wafers present. Such oxide growth might also occur from any trace amounts of water vapor present. SiO_2 or Si_3N_4 prevents such oxide growth.

The wafer is loaded into a quartz ampoule along with a few milligrams of red phosphorus. If the top layer is InGaAs, As is used instead of P. A P or As overpressure results which reduces surface decomposition. The ampoule is evacuated to $\sim 10^{-6}$ torr and sealed off with a torch. Various conditions have been used for the drive-in diffusion in order to move the p-n junction about 1 micron away from the substrate (Fig. 5(a)); a typical case is 2 hr at 700°C. The depth of the junction may readily be determined by using a delineation etch consisting of $50H_2O$: $6KOH:4K_3Fe(CN)_6$ (by weight). A cleaved cross-section is etched 10 sec under illumination from a 60-W light bulb (separated by about an inch). The cross-section is then examined under a Nomarski phase contrast microscope at 3776x magnification. Figure 6 shows such a cross-section.

After the diffusion, the SiO_2 or Si_3N_4 is removed. Typically when Si_3N_4 is grown on the layer side, some growth also occurs on the substrate side. It has been observed that this superfluous growth cannot be removed in HF or other etches, including aqua regia, unlike the growth on the top layer. We remove the stubborn nitride layer by using a dental sandblaster to gently remove part of the substrate. Sometimes a similar etch-resistant layer occurs on the substrate side when excessive As has been added to the diffusion ampoule. It too is sandblasted away.

Next (Fig. 5(a)), a 2000-Å Au-Zn layer is evaporated onto the substrate and alloyed. Pure Au forms a silver-colored com-

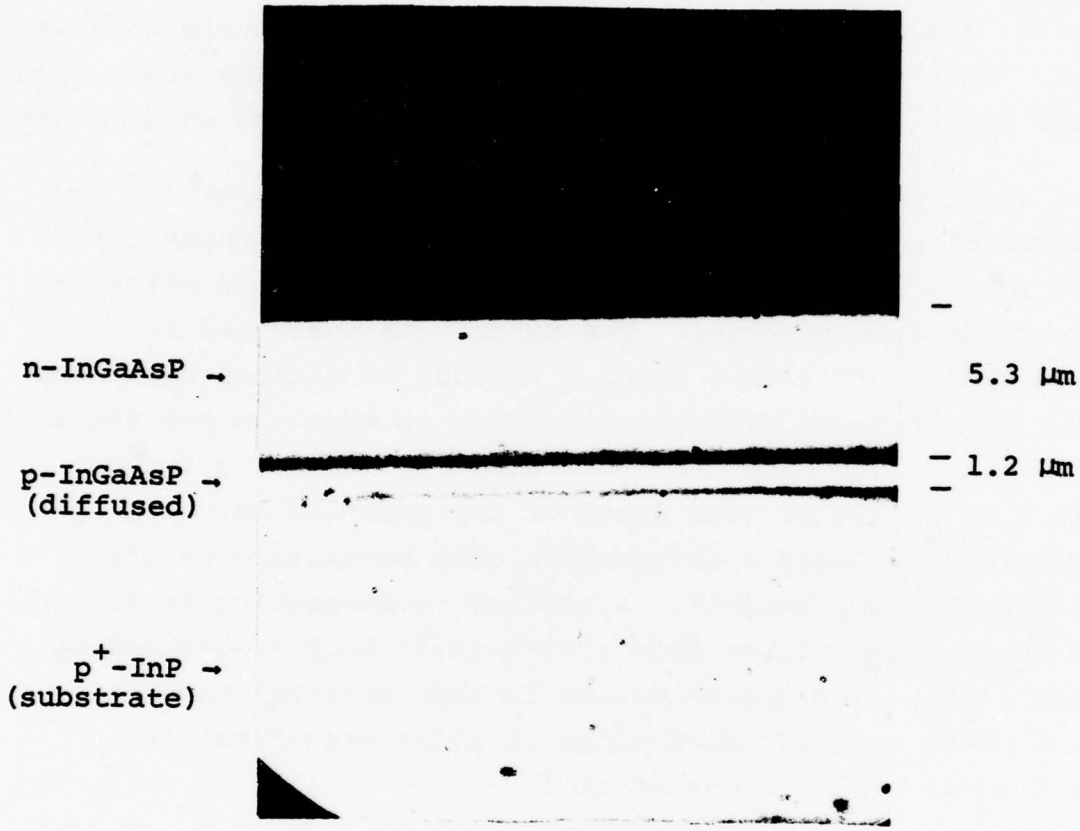


Fig. 6. P-N junction location after a drive-in diffusion.

pound with InP at temperatures over 475°C, and this temperature must be reached or exceeded to get a good ohmic contact.

Next, Shipley AZ-1350J photoresist is spun onto the layer side and 3-mil diameter holes (on 20-mil centers) are opened up in the resist. 1300 Å of Au-Sn are then evaporated over the layer. When the resist is dissolved in acetone, the Au-Sn metallization lifts away except where the 3 mil openings were. The Au-Sn dots are then alloyed at about 300°C.

Next (Fig. 5(b)), KTI-752 negative resist is used to define 6-12 mil diameter dots over the Au-Sn dots. The diameter used varies depending on what diameter is desired for the APD. Smaller diameter diodes result in higher yields and are thus preferred during the research stages. Ultimately 12-mil diameter diodes will be fabricated under this contract although currently 7-mil diameter diodes are the most common size made. Diodes smaller than 6 or 7 mils are difficult to probe and illuminate without illuminating beyond the edges (which would cause low values to be obtained in quantum efficiency measurements).

The wafer is then etched in 2% Br-methanol solution. The etch rate varies depending on stirring conditions, but is about 3 microns/min. Usually the wafers are etched so that the bottom of the mesa is a few microns into the InP rather than being marginally below the p-n junction. We have not noticed any performance differences between these approaches, and the former is much more reliable. Figures 7 and 8 show scanning electron microscope (SEM) pictures of mesas that have been etched somewhat longer than usual. Notice that the asymptotic slant (Fig. 8) is ~ 30° from the vertical rather than vertical so that the mesas still have enough slant to reduce the surface fields[10] compared to the bulk.

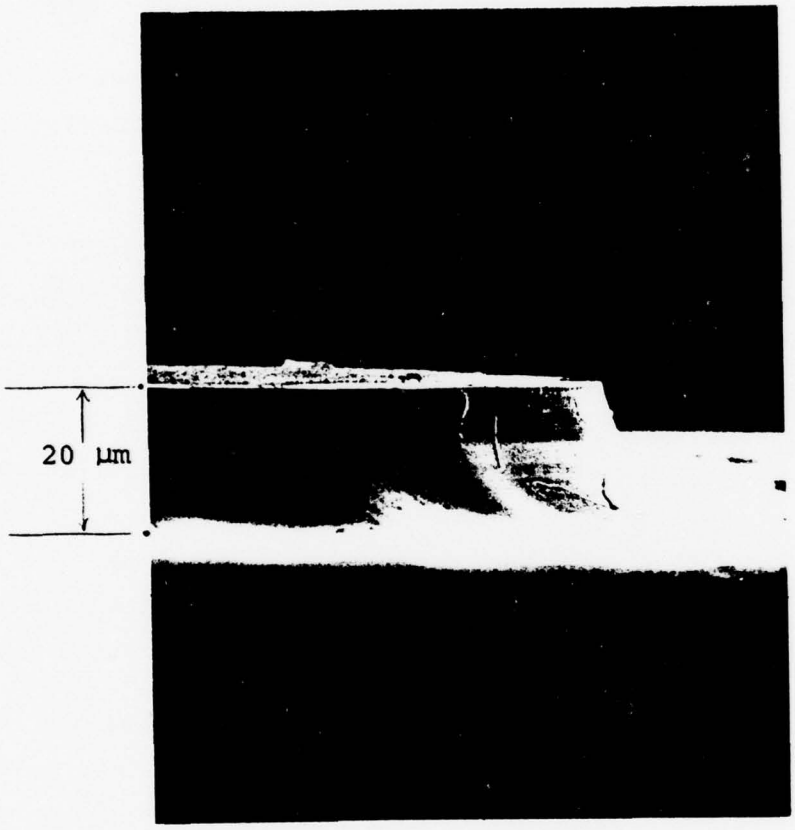


Fig. 7. Mesa etched in 2% Br-methanol.

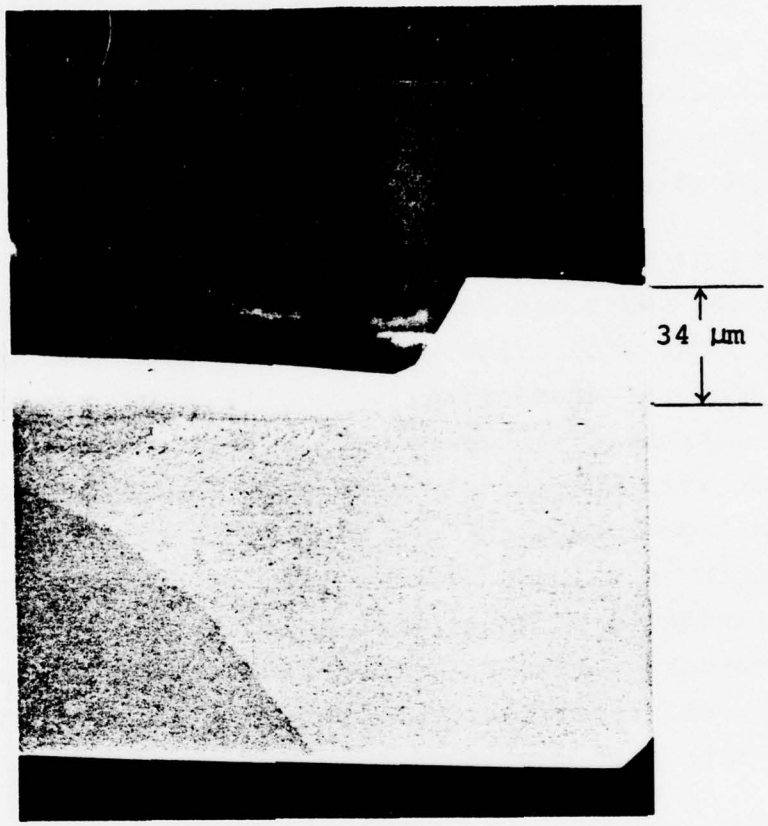


Fig. 8. Cross-section after long mesa-etch in Br-methanol. Note the non-vertical sides.

After the mesas are etched the photoresist is removed and attempts may be made to passivate the surface. Surface oxides (e.g. caused by etching in oxidizing etches such as H_2O_2/H_2SO_4 mixtures, or by SiO_2 deposition) are disastrous and should be avoided. However, leakage currents for a 7-mil diameter diode have been observed down to less than 5 nA up to 70% of the breakdown voltage. Above this point the leakage current rises rapidly and is probably the cause of the gain limitation that is observed (discussed later). Guard rings are probably needed.

At this point the diodes on the wafer are ready for testing. Typically all tests are done while the diodes are still on the wafer. A mount with a 200-MHz bandwidth has been constructed for this purpose. Occasionally we will want to mount individual diodes in microwave packages. If this is desired, a 1-micron layer of Au will be electroplated onto the alloyed contacts by conventional photochemical and plating techniques. The wafer will be diced up using a diamond saw. The tests performed include measurements of gain, gain uniformity, breakdown voltage, leakage current, series resistance, frequency response, quantum efficiency, and capacitance vs voltage. Preliminary noise measurements have also been performed.

The more precise optical measurements employ in-house quaternary lasers or LEDs. Originally lens optics were used, although now optical fibers have replaced them and are much easier to use. Graded index fiber with a 62-micron core and 5-mil outer diameter is used. The end of the fiber feeding the detector has been tapered to an outer diameter of 1-2 mils by drawing the fiber in a hydrogen flame before cleaving it. At a separation of about 1 mil the spot size on the diode surface is about 2 mils. Precision x-y-z manipulators are used on an optical table to make the alignment easy when observed under a Bausch and Lomb stereozoom microscope. The manipulators read in tenths of mils and may be used in conjunction with the fiber to test the spatial uniformity of gain on an APD.

3. RESULTS AND DISCUSSION

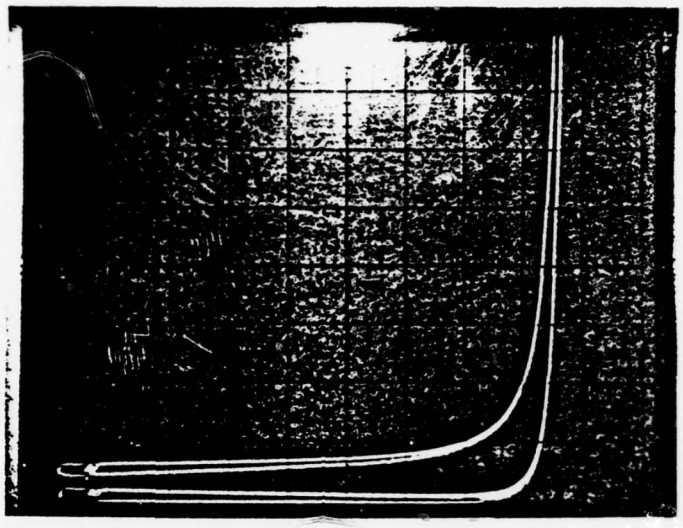
3.1 Device Characteristics

A good quaternary APD (according to the present level of achievement) has an I-V characteristic as shown in Fig. 9(a)-(d), all of which refer to the same 7-mil diameter diode. In Fig. 9(a) the reverse-biased part of the characteristic is shown in the dark (lower curve), and under illumination (upper curve) provided by a white microscope light. In Fig. 9(b) the dark current is shown on a more sensitive current scale, 5 nA/division; the voltage scale has not changed from Fig. 9(a) and is 10 V/division. Note that the dark current is below 5 nA until about 70% of the breakdown voltage, and then increases rapidly. At low voltages the dark current is less than 1 nA (the zero has been raised slightly above the baseline for clarity). For an untreated surface a good diode would have a vertical edge on the 5-nA current scale of Fig. 9(b) at 1/3 to 1/2 the breakdown voltage instead of 3/4 of the breakdown voltage as in 9(b). This suggests that the surface is one of the weak points of the present APDs. Figure 9(c) shows pairs of light on/off points for the same diode under the same illumination as in Fig. 9(a). The gain at higher biases is given by the separation of a pair of points at higher bias divided by the separation at lower biases. This is an approximation for the diode shown since the collection efficiency is not constant but increases slowly with increasing bias. A better approximation would estimate the unmultiplied photocurrent at high biases by making a linear extrapolation of the photocurrent at low biases. (Effectively one can simplify this procedure for this particular diode by using the photocurrent at ~ 60 V as the "low bias" value--see Fig. 9(a), top curve.)

Figure 9(d) is similar to 9(c) and has the same illumination. The larger current scale in Fig. 9(d) allows higher voltages to be viewed. Figure 9(c) shows that a gain of 2.5 occurs at a dark

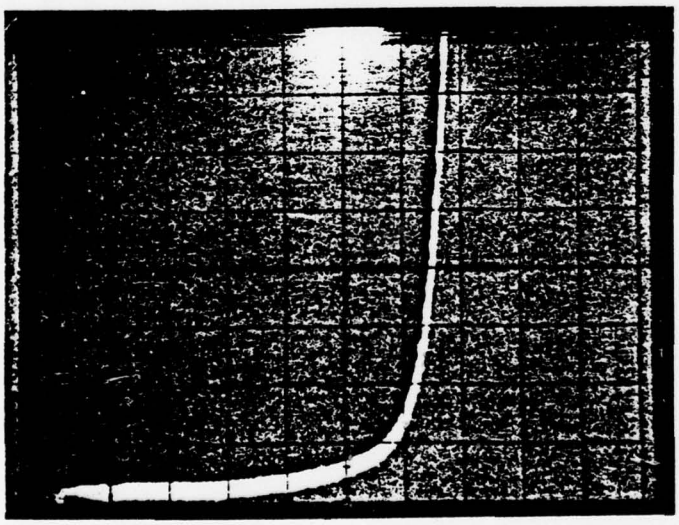
Top curve - under illumination

Lower curve - in the dark



(a)

Current (5 μA/div)



(b)

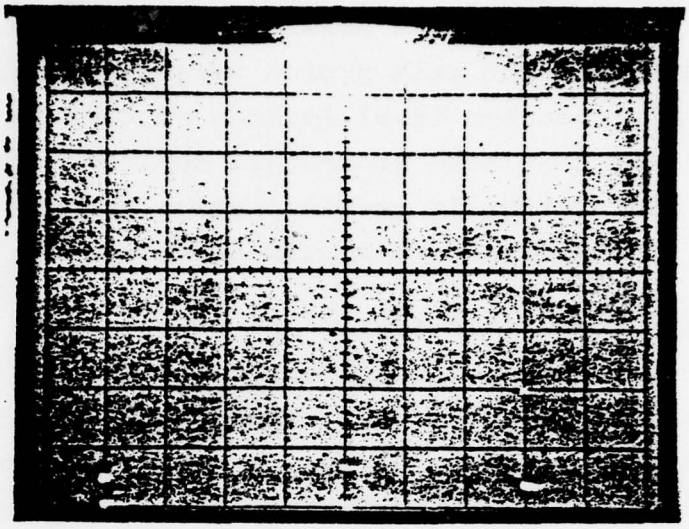
Dark Current (5 nA/div)

Reverse Bias (10 V/div)

Fig. 9. InGaAsP APD I-V characteristic.

Light on-off pairs

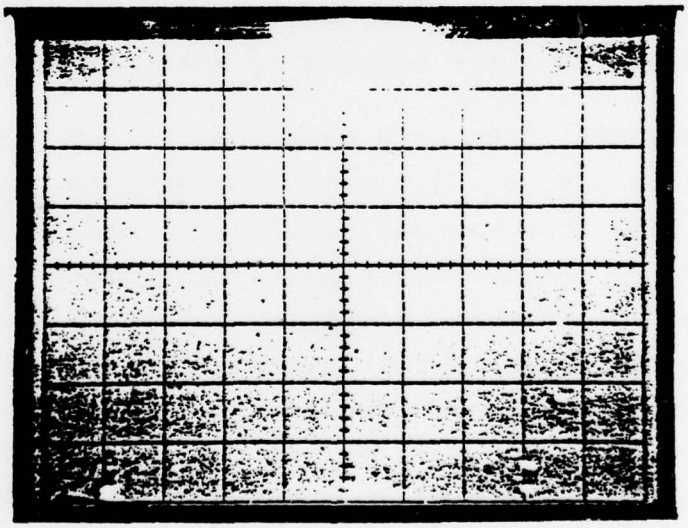
Current (5 μA/div)



(c)

Light on-off pairs

Current (20 μA/div)



(d)

Reverse Bias (10 V/div)

Fig. 9. (Contd.)

current of 2 μA and a gain of 5 at a dark current of 18 μA. With Fig. 9(d) one sees that to get a gain of about 9 requires about 70 μA of dark current. As we shall see, the large values of dark current in the avalanche gain region severely degrade the device performance. The nanoamp level leakage at half or less of the breakdown voltage that some groups are fond of reporting is irrelevant and misleading; it is the leakage current as a function of gain that is important and should be monitored.

Gains observed on a 60 cycles/sec curve tracer can be misleading. Surface charge storage and local thermal effects can lead to indications of high low frequency gain that does not persist at frequencies above ~ 1 kHz. In work completed before the initiation of this contract we had seen low frequency gains as high as 200--but the gain for a 100 μsec pulse was less than one. In that particular case the mesas had "negative" bevels (no longer the case) so that surface fields were actually enhanced,[10] and edge breakdown dominated. With experience, one can identify most cases of anomalous gain just by using a curve tracer, however there is no substitute for looking at the gain of short pulses.

Figure 10 shows pulse gain measurements for a diode similar to that shown in Fig. 9. A 1.1-micron emitting LED with a 5-10 nsec rise or fall time was pulsed with 0.5-nsec rise/fall time voltage pulses of 10-nsec duration. Measurements with a 320-psec rise/fall time Varian photomultiplier tube have shown that the rise and (slightly longer) fall times in Fig. 10 are those of the LED, and are in the 5-10 nsec range (indicative of ≈ 50 MHz bandwidth). The pulse height at low (60-V) biases (Fig. 10(b)) represents a photocurrent of 2 μA while at high (87.0 V) biases (Fig. 10(d)) the pulse height is 15 times this. The leakage current at this point where the gain is 15 was large--80 μA. Somewhat more gain could have been achieved at increased risk of burning out the diode. Typically, however, the gain saturates

(a) V = 87.0 V
LED is pulsed but light is blocked. The noise is rf pick-up.

(b) V = 60.0 V
Here the low bias gain is 1 and the photocurrent is 2 μA.

(c) V = 86.5 V
The gain is 11. The multiplied photocurrent is 22 μA.

(d) V = 87.0 V
Note the scale change. The multiplied photocurrent is 30 μA. The gain is 15.

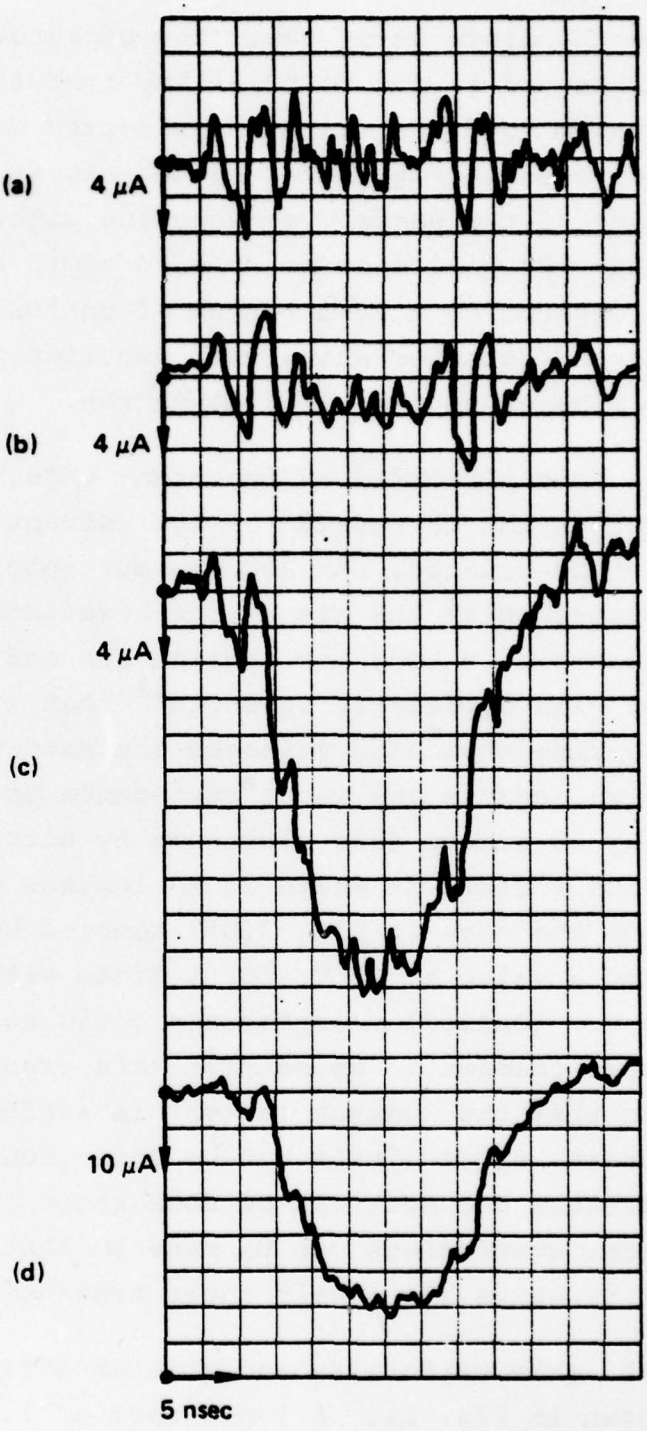


Figure 10. APD response to a pulsed 1.1-micron LED. Pulses are negative-going. Rise and fall times are those of the LED.

before the diode burns out. The background noise level is considerable and is due to rf pickup from the pulse generator and the 50-ohm load that is used in series with the LED. This is demonstrated in Fig. 10(a) by the excess noise that occurs at the time of the pulse even when the light from the LED has been blocked. We will soon be able to avoid the rf pickup problem by incorporating a 20-m length of optical fiber between the source and detector which will function as a 100-nsec optical delay line of negligible attenuation.

We have performed an important experiment that further indicates that the increased leakage current in the breakdown region is surface related. An APD was put into a chamber that could be pressurized with the gas sulfur hexafluoride, SF_6, and its I-V was observed in both the ambient air and in the SF_6. SF_6 is a gas of high dielectric strength[11] that is sometimes used to prevent arcing when high voltages are needed. It is a very electronegative, stable gas whose resistance to breakdown is due to its ability to remove free electrons by attachment.[11] It was found that the voltage at which 20 nA leakage occurred (e.g. the location of the edge in Fig. 9(b)) doubled by using the SF_6 and reached a value of 37 V, for a diode with a breakdown voltage of 45 V. (Optical measurements could not be performed in the enclosed chamber.) We believe this experiment is a strong indication that the leakage current is surface dominated. This is fortunate, since little can be done about fundamental material limitations but much can be done about surface problems. In particular, guard rings can be made so that exposed surfaces need never be above about half their breakdown voltage.

The gain uniformity and quantum efficiency of another diode is shown in Fig. 11. A 2-mil spot of 1.05-micron light has been scanned across an arbitrary chord of the circular APD surface. Note that the gain is bulk rather than simply surface gain. The

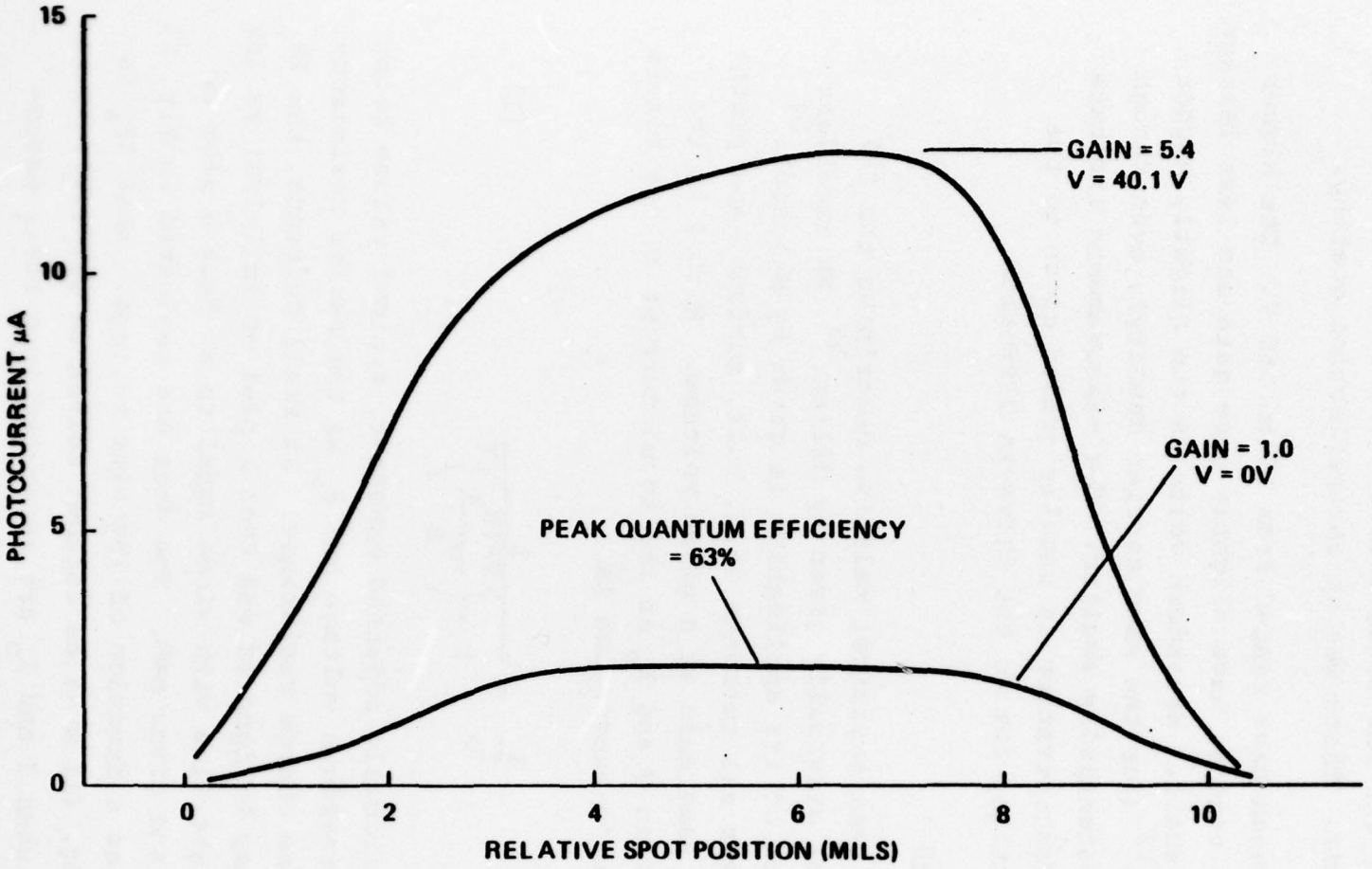


Figure 11. InGaAsP gain uniformity at λ = 1.05 microns.

quantum efficiency of the unbiased diode (which has an InP capping layer) is 63%, and was determined by comparison with a calibrated Ge photodiode. There was no antireflection coating.

Breakdown voltages have ranged from 25 to 160 V. The higher breakdown voltages tend to have slightly more gain and less leakage but the effect is small. Breakdown voltages run slightly higher than those in GaAs[12] (for the same carrier density), even though the bandgap is substantially smaller. C-V measurements indicate that the carrier concentration is usually graded close to the center of the junction, due to the drive-in diffusion.

3.2 Gain Saturation

A very useful semi-empirical relation describing the I-V curve of an APD was originally given by Miller.[13] An excellent detailed discussion of its application is given by Melchior.[14] In the simplest case all currents (e.g. bulk, surface, and photocurrent) have the same gain at a given voltage. With I as the total current at bias V and I_o as the total current at low biases (where M=1), Miller's expression is

$$\frac{I}{I_o} = \frac{1}{1 - \left(\frac{V-IR_s}{V_B}\right)^n} \qquad (1)$$

where n is an empirically adjusted constant, typical values being 2-6. V_B is the breakdown voltage and R_s is the series resistance, including any space charge resistance. At small currents, the IR_s term on the RHS may be ignored and then a plot of ln(1-1/M) vs lnV should be a straight line with slope equal to n. Such a plot is shown in Fig. 12 and gives n≈5. The data are replotted in Fig. 13 to show the gain as a function of the bias voltage. When IR_s is not negligible, Eq. (1) must be further solved to get I(V). When this is done and when I and I_o are separated into their photo-

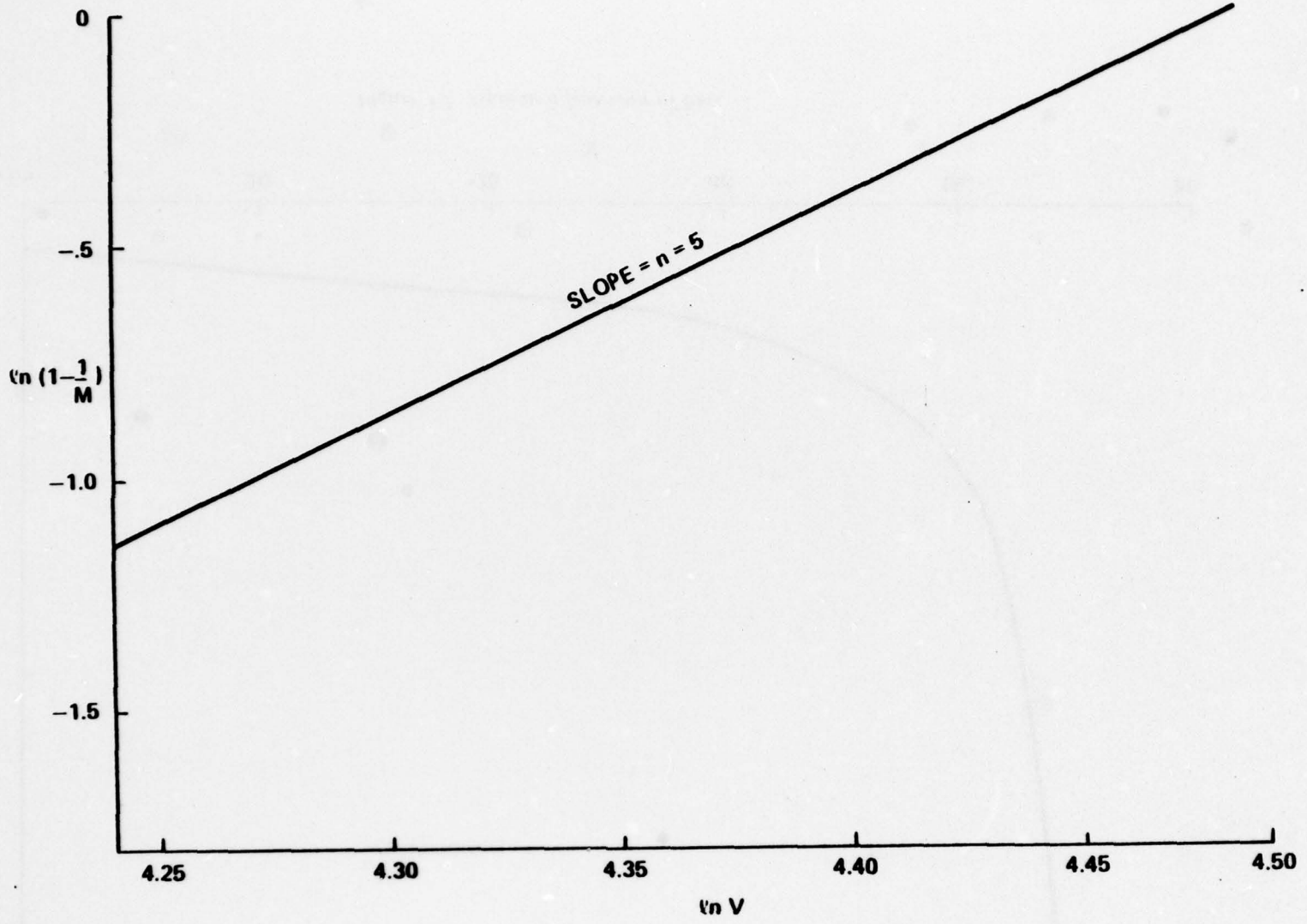


Figure 12. Determination of Miller's n.

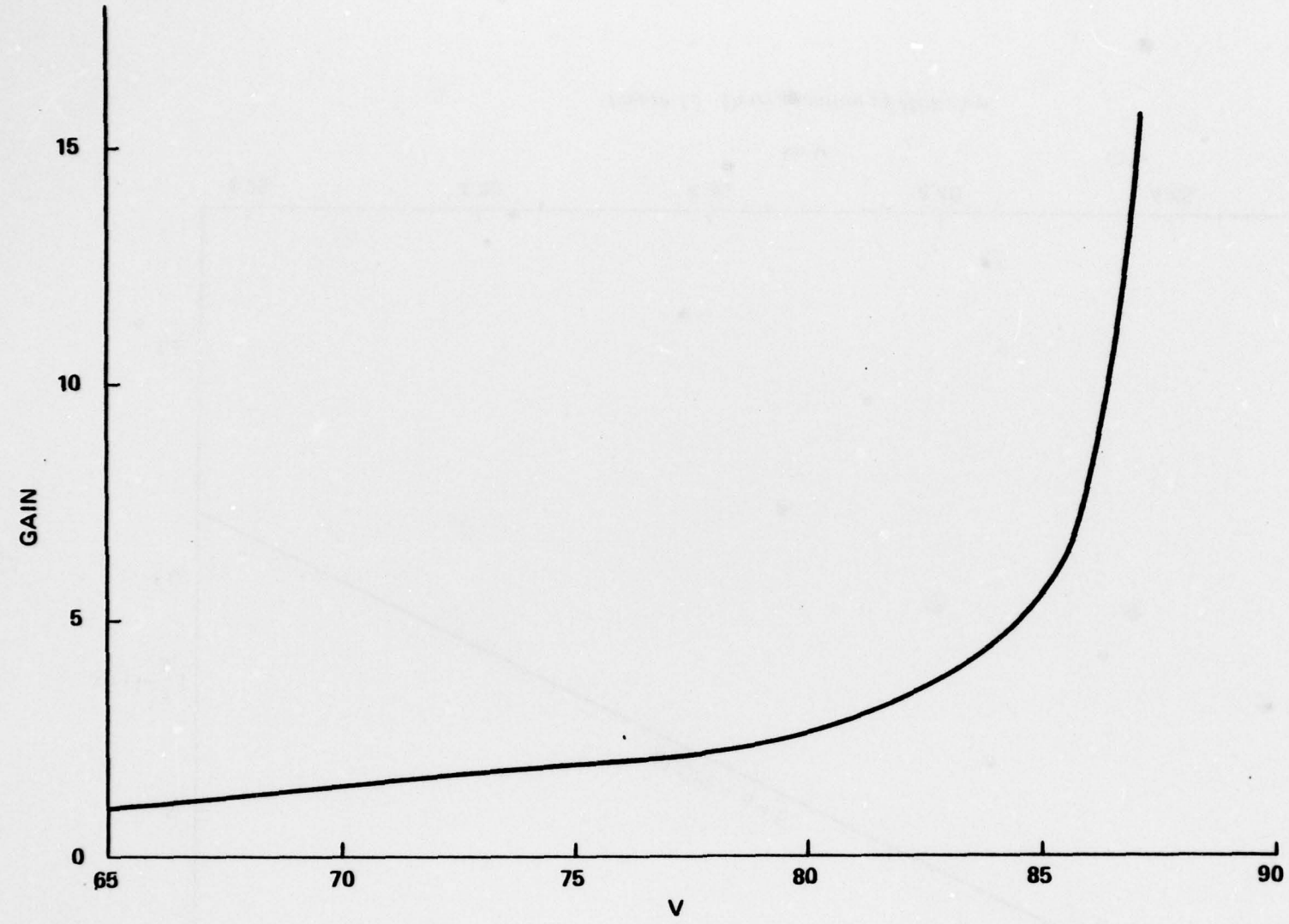


Figure 13. Gain as a function of bias.

current and dark current components, one finds that the photocurrent gain goes through a maximum value at $V=V_B$ and then actually decreases. The maximum gain is given by

$$M_{max} = \sqrt{\frac{V_B}{nR_s I_o}} \quad . \tag{2}$$

R_s for a local "hot" spot tends to be about 10^4 ohms[15] and is primarily due to the screening effect of a large density of electrons. I_o is hard to choose, but for an unmultiplied photocurrent of 1 μA, I_o = 1 μA is a lower limit. With V_B = 50 V, n = 5, R_s = 10^4 ohms, and I_o = 1 μA, one finds $M_{max} \approx 30$. Hence the gain saturation that is often observed may be at least qualitatively understood. The gain saturation arises from the IR_s term in Eq. (1). To minimize this term one must keep R_s small by eliminating localized breakdown, and keep I small by controlling bulk and surface leakage. The guard ring structures that we are beginning to work on may solve these problems.

3.3 The Effects of Leakage Current

In the previous section we have discussed how leakage current can lead to gain saturation. One can demonstrate this on a curve tracer by using large values for the series limiting resistance. Typically one finds that for a resistance larger than a few thousand ohms the maximum gain achievable is reduced. The large leakage current in the avalanche gain region is the cause. As we have mentioned, the surface is believed to dominate the leakage current and the guard rings that we are developing are expected to be a great help.

Another effect the leakage current has is to cause noise. The shot noise current rms value, I_n, in a 3-dB bandwidth of Δf (cycles/sec) may be expressed as

$$I_n^2 = \pi e\,(\Delta f)\,(FM)\,I \tag{3}$$

where I is the dc component of the multiplied current, M the current gain, and F the excess noise factor. F varies between 1 and M, depending, in part, on the ratio of the electron and hole ionization coefficients. For a nonavalanching diode, Eq. (3) is simply the usual shot noise expression having F=M=1. In Eq. (3) we have assumed the measuring apparatus has a high frequency roll-off of 3 dB per octave of current, so that the noise bandwidth is $(\pi/2)\,\Delta f$, where Δf is the 3 dB signal bandwidth.

Leakage current per se is not that noisy. If the leakage current is just shunt leakage having F=M=1, then the noise in a 100-MHz bandwidth caused by 1 μA of leakage is 7 nA. The equivalent input noise current of the best 100-MHz transimpedance preamplifier that is likely to be developed is at least 10 nA so that even 1 μA of "well-behaved" leakage current may be tolerable. The noise current, Eq. (3), is plotted in Fig. 14, for different values of FM. A Ge APD has F≈M so that if the same 1 μA of leakage had come from multiplication of 0.1 μA initial current, then M=F=10 and the noise current would be 70 nA rather than 7 nA--a ten-fold increase in the noise current for the same value of leakage current. Hence the quality of the leakage current is as important as the quantity.

We have performed some preliminary noise measurements on one of our APDs. The APD was biased into the avalanche gain region and the dark current fed into a low nosie preamp (Texas Instruments TIXL150) having an equivalent input noise current of about 0.1 μA, and a 100-MHz bandwidth. The output of the preamp was further amplified and fed into a spectrum analyzer. It was observed that our leakage current is noise (FM >> 1). In particular, at a dark current of 8 μA the dark current noise equalled the preamp noise. At this point the gain was about 3-4. Though the diode was capable of gains up to 15, it would not be advantageous to operate above a gain of 3-4 because of noise and sensitivity considerations. Again we find that much may be gained if a guard ring can be constructed to substantially reduce leakage current.

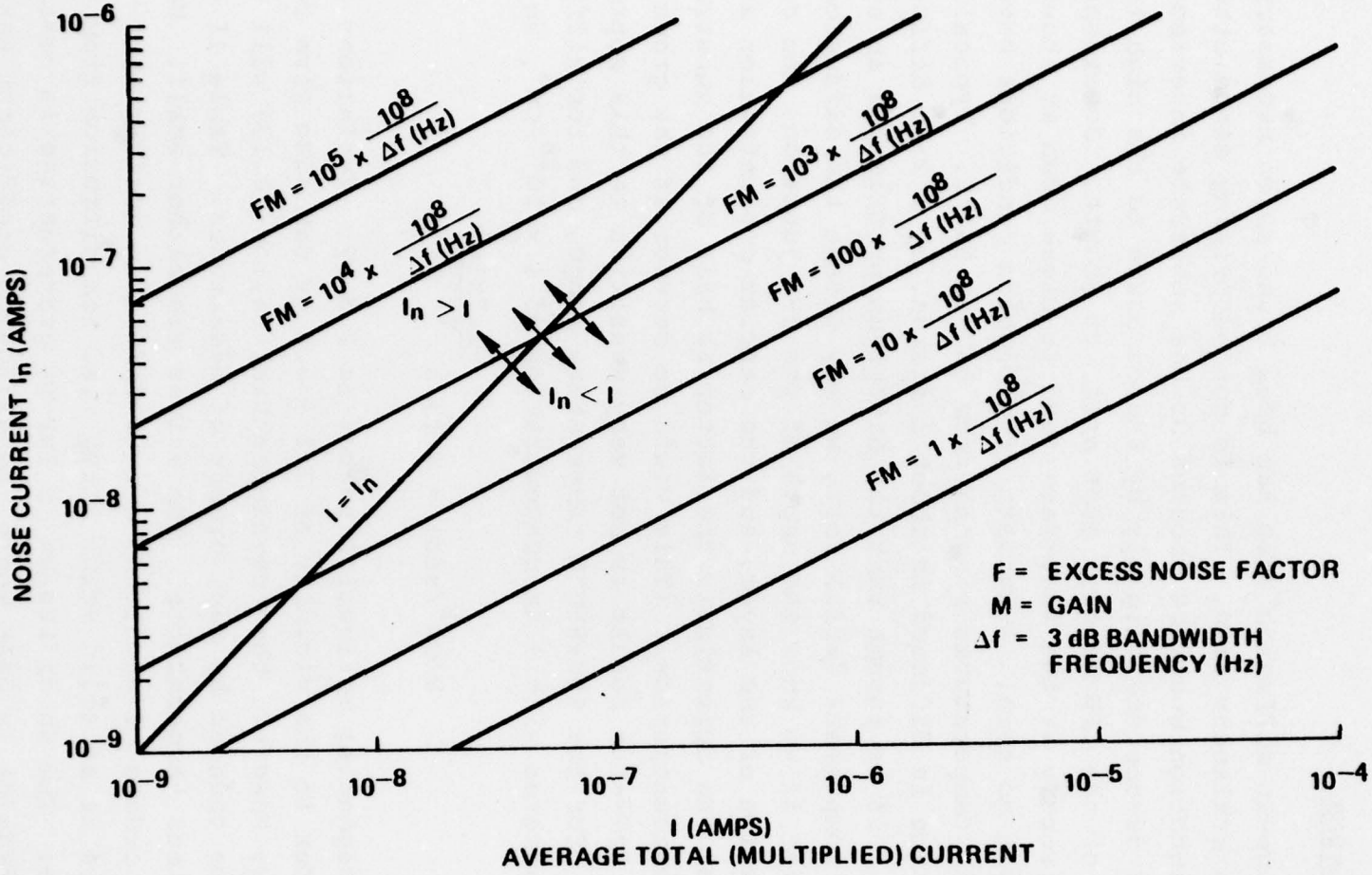


Figure 14. Noise current vs total current for different gain and excess noise factor values.

3.4 Diffusion

A drive-in diffusion step has been found to be necessary for obtaining avalanche gain. This is not surprising since otherwise the p-n junction would be located at the substrate interface, which has decomposed slightly by the exposure to the high temperatures of the LPE reactor just prior to growth. Junctions formed directly at the interface tend to break down at about 5 V and exhibit no gain. A variety of diffusion conditions have been tried with temperatures ranging from 650 to 850°C. Typically the junction is diffused in about 1 micron, by a 2-hr diffusion at 700°C. If we assume that the diffusion profile has an error function complement (erfc) form, we may obtain the diffusion coefficient if we know the depth of the p-n junction, the carrier concentration of the layer, and the carrier concentration at the interface. We approximate the latter as half of the substrate carrier concentration. (This would be correct if the grown layer was also InP--the result is not very sensitive to this approximation.) For the 650-850°C temperature range, and for diffusion from substrates with a Zn concentration of $1 \times 10^{18}/cm^3$, we find

$$D(cm^2/sec) = 0.13\, e^{\frac{-2.7 \times 10^4}{T(°K)}} \quad . \qquad (4)$$

The corresponding activation energy is 2.3 eV. Variations of this number in the vicinity of 2.1 $\pm$ 0.4 eV can also give reasonable fits; however, the pre-exponential factor (0.13) will then have to be changed by many orders of magnitudes. Table II gives D at various temperatures. The values are rather small. We have observed orders of magnitude larger diffusion coefficients when the source is at solid solubility, i.e. for diffusion from a vapor Zn source. The Zn diffusion in InP or quaternaries is reminiscent of Zn diffusion in GaAs where the diffusion coefficient varies by 5 orders of magnitude[17] depending on concentration.

TABLE II

Zinc Diffusion Coefficients for Diffusion from a $1 \times 10^{18}/cm^3$ Zn-Doped InP Substrate

T(°C)	D (cm^2/sec)
650	2.6×10^{-14}
750	4.5×10^{-13}
850	4.7×10^{-12}

In the fabrication of guard ring structures we need to know the doping gradient at the position of the junction in order to determine the breakdown voltage. A proper design would have the breakdown voltage at the edge of the guard ring be considerably larger than the breakdown voltage in the primary junction region. For an infinite source, erfc diffusion we have derived that the doping gradient and junction depth are given approximately by

$$\left.\frac{dN}{dx}\right|_{x_j} \approx \frac{-n}{\sqrt{Dt}} \sqrt{\ln\left(\frac{N_o}{n}\right)} \tag{5}$$

$$x_j \approx 2\sqrt{Dt}\left[\sqrt{\ln\left(\frac{N_o}{n}\right)} - 0.3\right] . \tag{6}$$

Here n is the carrier concentration of the layer and N_o is the concentration at the source/layer interface. Equations (5) and (6) apply for the case of diffusion from a doped semiconductor layer of at least moderate thickness. The approximation is good for $N_o/n \geq 2$.

Another type of diffusion profile that is of interest is the Gaussian profile, which results from diffusion from a limited source. Such a profile would apply to the case of a two-step diffusion consisting of a predeposition followed by drive-in. In this case it is easy to show that the doping gradient at the junction and the junction depth are given by

$$\left.\frac{dN_2}{dx}\right|_{x_j} = \frac{-n}{\sqrt{D_2 t_2}} \sqrt{\ln\left(\frac{N_{02}}{n}\right)} \tag{7}$$

$$x_j = 2\sqrt{D_2 t_2}\, \sqrt{\ln\left(\frac{N_{02}}{n}\right)} \tag{8}$$

where N_{02} is the final surface concentration. For a two-step diffusion[16] having $\sqrt{D_1 t_1} \ll \sqrt{D_2 t_2}$ and a surface concentration N_{01}, N_{02} is given by

$$N_{02} \approx \frac{2N_{01}}{\pi} \left(\frac{D_1 t_1}{D_2 t_2}\right)^{1/2} . \tag{9}$$

Comparison of Eqs. (5)-(8) shows that for a given final surface concentration the doping gradient at the junction will be approximately the same for both types of diffusion; the main difference will be that the Gaussian diffusion will have the junction about $0.6\sqrt{Dt}$ deeper than the erfc diffusion.

With Sze's values[12] of breakdown voltages for graded junctions Eqs. (5)-(8) can be used to show that convenient conditions exist to double the breakdown voltage at the guard ring compared to the breakdown voltage of the primary junction region.

4. FUTURE PLANS

There are more detailed data that will be taken in order to fully characterize the APDs. For example, in-house pulsed laser sources (at 1.3 microns) will be used to obtain a higher lower limit on the APD bandwidths than is presently possible using the LED sources. However, the development of the optimum structure for the APDs is still the highest priority and so these more refined measurements will probably be taken somewhat later.

Probably the most important thing that needs to be done is to develop processes for making the required guard rings. These will be made by some method of selective diffusion that is yet to be worked out. Problems include determining sizes of diffusion coefficients, determination and control of surface concentrations, minimization of surface decomposition, further study of protective and masking capping layers (e.g. SiO_2, Si_3N_4, InP), and avoidance of undesired impurities. We will begin using Zn as a dopant since we are more familiar with it. However, the p-type dopants Cd, Hg, and Mg will also be considered as will be the n-type dopants S, Si, Sn, and Te. It is hoped that both fast and slow diffusants may be found, as this allows greater flexibility in the methods of guard ring construction.

Once we have fabricated good guard ring APDs, we will determine whether electrons or holes have the higher ionization coefficient. This knowledge is important since if holes have the higher ionization coefficient, for example, the proper structure would have the light absorbed on the n-type side of the junction. However, reliable ionization coefficients cannot be determined without a high quality APD.

More work will also be done on the materials side. Lower dislocation density n-type substrates are hoped for (p-type substrates have nearly zero dislocation density). Higher purity

layers with less compensation are also desired. Structures with p-type rather than n-type active regions should be grown. Furthermore, the orientation dependence of the ionization coefficients may require growth on orientations other than the (100) orientation that is presently used.

5. REFERENCES

1. J. Conradi, F. P. Kapron, J. C. Dyment, IEEE Trans. ED-25, 180 (1978).

2. G. A. Antypas and R. L. Moon, J. Electrochem. Soc. 120, 1574 (1973).

3. R. Sankaran, R. L. Moon, and G. A. Antypas, J. Cryst. Growth 33, 271 (1976).

4. R. Sankaran, G. A. Antypas, R. L. Moon, J. S. Escher, and L. W. James, J. Vac. Sci. Technol. 13, 932 (1976).

5. Y. Takeda, A. Sasaki, Y. Imamura, and T. Takeda, J. Appl. Phys. 47, 5404 (1976).

6. H. Nagai and Y. Noguchi, Appl. Phys. Lett. 29, 740 (1976).

7. S. B. Hyder, G. A. Antypas, J. S. Escher, and P. E. Gregory, Appl. Phys. Lett. 31, 551 (1977).

8. T. P. Pearsall, R. Bisaro, R. Ansel, and P. Merenda, Appl. Phys. Lett. 32, 497 (1978).

9. C. J. Nuese, R. E. Enstrom, and J. R. Appert, Device Research Conference, 1977 (unpublished).

10. R. L. Davies and F. E. Gentry, IEEE Trans. ED-11, 313 (1964).

11. J. G. Trump in Dielectric Materials and Applications, A. Von Hippel, ed. (Technology Press of MIT, 1954), p. 149.

12. S. M. Sze, Physics of Semiconductor Devices (Wiley Interscience, NY, 1969).

13. S. L. Miller, Phys. Rev. 99, 1234 (1955).

14. H. Melchior, IEEE Trans. ED-13, 829 (1966).

15. A. G. Chynoweth, Semiconductors and Semimetals 4, 319 (1968).

16. B. Tuck, Introduction to Diffusion in Semiconductors (Peter Peregrinns LTD., Stevenage, England, 1974).

17. M. A. H. Kadhim and B. Tuck, J. Mater. Sci. 7, 68 (1972).